IN THE CLAIMS:

Please amend the claims as indicated below.

1. (Currently Amended) A method for reducing leakage current in a read only memory device comprised of an array of transistors having a plurality of columns of transistors, wherein said plurality of columns of transistors are arranged into a plurality of sub-arrays, comprising the step of:

precharging only a portion of said columns in one of said sub-arrays during a given read cycle of said read only memory device.

2. (Original) The method of claim 1, wherein said portion of said columns is limited to a subset of columns including those columns that will be read during said given read cycle.

3. (Original) The method of claim 1, further comprising the step of decoding a read column address to precharge only said portion of said columns that will be read during said given read cycle.

4. (Cancelled).

5. (Original) The method of claim 4, further comprising the step of selectively precharging one or more of said plurality of sub-arrays having columns that will be read during said given read cycle.

6. (Original) The method of claim 1, further comprising the step of precharging only those columns that will be read during said given read cycle.

7. (Currently Amended) A read only memory device, comprising:

an array of transistors having a plurality of columns of transistors wherein said plurality of columns of transistors are arranged into a plurality of sub-arrays; and

a decoder for selectively precharging only a portion of said columns in one of said sub-arrays during a given read cycle.

8. (Original) The read only memory device of claim 7, wherein said portion of said columns is limited to a subset of columns including those columns that will be read during said given read cycle.

9. (Original) The read only memory device of claim 7, further comprising a decoder to decode a read column address to precharge only said portion of said columns that will be read during said given read cycle.

10. (Cancelled).

11. (Original) The read only memory device of claim 10, further comprising a precharge decoder to selectively precharge one or more of said plurality of sub-arrays having columns that will be read during said given read cycle.

12. (Original) The read only memory device of claim 7, wherein said read only memory device is further configured to precharge only those columns that will be read during said given read cycle.

13. (Currently Amended) A method for reading a read only memory device having a plurality of columns of transistors arranged into a plurality of sub-arrays, comprising the step of:

precharging only a portion of said columns in one of said sub-arrays during a given read cycle of said read only memory device; and

evaluating said read only memory device during said given read cycle.

14. (Original) The method of claim 13, wherein said portion of said columns is limited to a subset of columns including those columns that will be read during said given read cycle.

15. (Original) The method of claim 13, further comprising the step of decoding a read column address to precharge only said portion of said columns that will be read during said given read cycle.

16. (Cancelled).

17. (Original) The method of claim 16, further comprising the step of selectively precharging one or more of said plurality of sub-arrays having columns that will be read during said given read cycle.

18. (Original) The method of claim 16, further comprising the step of precharging only those columns that will be read during said given read cycle.

19. (Currently Amended) An integrated circuit, comprising:

a read only memory device, comprising:

an array of transistors having a plurality of columns of transistors, wherein said plurality of columns of transistors are arranged into a plurality of sub-arrays; and

a decoder for selectively precharging only a portion of said columns in one of said sub-arrays during a given read cycle.

20. (Original) The integrated circuit of claim 19, wherein said portion of said columns is limited to a subset of columns including those columns that will be read during said given read cycle.

21. (Original) The integrated circuit of claim 19, further comprising a decoder to decode a read column address to precharge only said portion of said columns that will be read during said given read cycle.

22. (Cancelled).

23. (Original) The integrated circuit of claim 22, further comprising a precharge decoder to selectively precharge one or more of said plurality of sub-arrays having columns that will be read during said given read cycle.

24. (Original) The integrated circuit of claim 19, wherein said read only memory device is further configured to precharge only those columns that will be read during said given read cycle.

Please add the following new claim:

25. (New) The method of claim 1, wherein unselected columns in said plurality of columns of transistors are maintained at a ground potential.